REMARKS

Claims 32-68 are pending. Claim 1 has been amended. A marked-up version of this claim, showing changes made, is attached hereto as Appendix A. Applicants respectfully request reconsideration in light of the amendment and following remarks.

Claim 32 has been amended to positively recite the method step of "annealing the top conducting layer with an oxidizing gas anneal." Support is found in Applicants' specification, page 8, lines 8-10.

Claims 32-46 and 48-55 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Ochiai. Reconsideration is respectfully requested.

The claimed invention relates to the method of forming a capacitor structure by annealing the top conducting layer. Annealing the top conducting layer results in a capacitor structure with reduced capacitor current leakage relative to conventionally formed structures. The prior art did not teach or suggest annealing the top conductive layer. Applicants' method of forming a capacitor structure rectifies problems associated with prior art structures. In fact, Applicants' capacitor structure yields a current leakage density reduced by a factor of at least 10 over the prior art structures (Applicants' specification, FIG. 2, page 12, lines 2-4, and FIG. 3, page 13, lines 1-5).

As such, independent claim 32 recites a method of forming a capacitor comprising "forming a bottom conducting layer, forming a dielectric layer . . . forming a top conducting layer . . . and annealing the top conductor layer with an oxidizing gas anneal."

The Office Action asserts that Ochiai teaches "annealing the top conducting layer." (Office Action, page 2). In support, the Office Action cites Ochiai's FIGS. 3-6 and Col. 5, lines 33-55. Applicants respectfully submit that Ochiai fails to teach the step of annealing the top conducting layer. There is no support whatsoever in Ochiai, Col. 5, lines 33-55, for this assertion. In fact, there is no teaching anywhere in Ochiai that the top

conducting layer is annealed. Moreover, Ochiai does not teach using an "oxidizing gas anneal," as claim 32 further recites.

Ochiai simply teaches that the "lower electrode layer 18, a dielectric film 19 and an upper electrode layer 20 are stacked in this order." (Col. 5, lines 15-17). In fact, Ochiai teaches away from annealing any of the capacitor layers. Specifically, Ochiai teaches that "the lower electrode layer 18, the dielectric film 19 and the upper electrode layer 20 . . . are selectively removed and with the second interlevel insulator 17 as an end point detection layer, at the same time, the surface is flattened using CMP method." (Col. 7, lines 16-21) (emphasis added). Ochiai does not teach annealing the top conducting layer, much less the method step of "annealing the top conductor layer with an oxidizing gas anneal," as claim 32 recites (emphasis added).

Accordingly, for at least these reasons, withdrawal of the rejection for claim 32 is solicited. In addition, dependent claims 33-46 and 48-55 which depend from and incorporate all of the limitations of independent claim 32, are similarly allowable for at least the reasons provided above regarding claim 32.

Moreover, Ochiai does not teach a method of forming a capacitor comprising "depositing an oxygen barrier over said conductive plug prior to forming the bottom conducting layer," as claim 33 recites (emphasis added). Ochiai teaches forming a "mutual-diffusion-preventing area 17A using N_2 . . . by applying N_2 (Nitrogen) onto each surface of the trenches." (Col. 5, lines 26-28) (emphasis added). This is an additional reason for the allowance of claim 33.

Ochiai does not teach a method of forming a capacitor comprising "annealing the dielectric layer," as claim 34 recites. In fact, as discussed previously, Ochiai does not teach whatsoever the step of annealing any layer of the capacitors. This is an additional reason for the allowance of claim 34.

Ochiai does not teach a method of forming a capacitor wherein the "top conducting layer is formed of a non-oxidizing material permeable to oxygen," as claim 49

recites. This is an additional reason for the allowance of claim 49.

Ochiai does not teach a method of forming a capacitor wherein the "top conducting layer is formed of a conducting metal oxide," as claim 50 recites. Ochiai does not teach that the conducting layer can be a metal oxide. In fact, Ochiai only teaches that the upper electrode can be formed of platinum or "other metal materials such as, Ir (Iridium), Ru (Ruthenium), Rh (Rhodium), Pd (Palladium) can be used." (Col. 5, lines 35-37). This is an additional reason for the allowance of claim 50.

Claims 47 and 56-68 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ochiai in view of Hirota. Reconsideration is respectfully requested.

Hirota is not properly combinable with Ochiai because the cited references are directed to solving completely different problems. Ochiai provides a method of forming a "capacitor having a structure with a flat surface comprising the edges of the lower electrode layer and the dielectric film, and the upper electrode layer is formed in the trench of the second interlevel insulator respectively." (Abstract). Employing Ochiai's methods result in a capacitor structure that does not have "hard-to-remove deposits and a dirt made from a mixture of resist and platinum pile-up when ion milling etching is applied." (Col. 2, lines 20-25). Accordingly, Ochiai's " lower electrode layer, the dielectric film and the upper electrode layer are processed collectively." (Abstract) (emphasis added).

In contrast, Hirota is directed to providing a "double-layered tantalum oxide film serving as a capacitance insulation film." (Abstract). There is simply no motivation to combine the two references. Ochiai teaches processing the lower electrode, the dielectric film, and the upper electrode layers simultaneously. Hirota teaches a plurality of steps to process the dielectric layer separate from processing the lower and upper electrode layers. (Col. 15, lines 64-67 – Col. 17, lines 1-26). Moreover, neither Ochiai nor Hirota teaches or suggests annealing the top conductive layer, much less, annealing the top conductive layer with an oxidizing gas anneal.

Even assuming arguendo that the cited references might be combinable, which they are not, one still would not obtain Applicants' claimed invention. The cited references do not teach or suggest a method of forming a capacitor comprising "forming a bottom conducting layer, forming a dielectric layer . . . forming a top conducting layer . . . and annealing the top conductor layer with an oxidizing gas anneal," as claim 32 recites.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By_____

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APPENDIX A

32. (amended) A method of forming a capacitor in a semiconductor device, said method comprising:

forming a bottom conducting layer;

forming a dielectric layer formed over the bottom conducting layer;

forming a top conducting layer over the dielectric layer; and

annealing the top conducting layer with an oxidizing gas anneal [after it is formed].